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EXAMINER	
SHARON, AYAL I	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/060,750	DEVINS ET AL.	
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-34 of U.S. Application 10/060,750 filed on 01/30/2002 are currently pending.
2. In Applicants' response filed 11/23/05, no claims were amended, no claims were cancelled, and no claims were added.

Drawings

3. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. The prior art used for these rejections is as follows:

6. Blaner, B. et al. "An Embedded PowerPC™ SOC for Test and Measurement Applications." 13th Annual IEEE Int'l ASIC/SOC Conf., 2000. Sept. 13-16, 2000. pp.204-208. (Henceforth referred to as "**Blaner**").

7. Devins et al., U.S. Patent 6,487,699. (Henceforth referred to as "**Devins**"). Examiner notes that the issued patent has a different inventive entity.

8. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

9. **Claims 1-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Blaner.**

10. In regards to Claim 1, Blaner teaches the following limitations:

1. A verification test bench system for testing a system-on-a-chip (SOC) interface of an SOC, said verification test bench system comprising:

a verification interface model connected to said SOC interface; and

> (See Blaner, especially: p.208, "E. Verification Testbench")
>
> Blaner teaches (See "E. Verification Testbench". Emphasis added): "To accomplish this synchronization, ***a memory-mapped external device*** containing software readable and writable registers that appear as wires in the testbench ***is connected to the external bus***."

a test bench external bus interface unit (EBIU) connected to said verification interface model, wherein said test bench EBIU is connected to a SOC EBIU within said SOC.

> (See Blaner, especially: p.205, "II. SOC Structure")
>
> Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called***

the external bus master, to take ownership of the external bus and access attached memories."

Moreover, Fig.2 of Blaner (see p.205), shows an EBIU in the extreme upper-left corner of the SOC block diagram. This diagram shows that the SOC EBIU connects externally to "SRAM, Flash, ROM, and 'External Master'".

While Blaner does not expressly teach that the "off-chip device, called the external bus master" also uses an EBIU in order to connect to the SOC's EBIU, examiner finds this to be inherent because:

(1) The two ends of an interface must match (e.g. electrical plug and socket, phone jack and socket, parallel port plugs and sockets, etc.), otherwise the interface does not work properly. This applies also to the external buses on SOCs, and

(2) Blaner teaches (See "E. Verification Testbench"): "System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench." A complete system verification must also include a verification of the EBIU on the SOC, therefore the testbench must have an interface compatible with the SOC EBIU.

11. In regards to Claim 2, Blaner teaches the following limitations:

2.The verification test bench system in claim 1, wherein said SOC EBIU allows a test case running in said SOC to control both said SOC interface and said verification interface model.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

12. In regards to Claim 3, Blaner teaches the following limitations:

3.The verification test bench system in claim 1, wherein said SOC interface and said verification interface model are programmed by a test case running in said SOC.

(See Blaner, especially: p.205, "II. SOC Structure" and p.208, "E. Verification Testbench")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

Blaner also teaches (See "E. Verification Testbench". Emphasis added): "Wrap backs are utilized as much as possible, and behaviorals often contain hard-coded packet or stream data."

Examiner interprets that "Wrap backs" do not containing functioning processors, and therefore must rely on the SOC processor.

13. In regards to Claim 4, Blaner teaches the following limitations:

4.The verification test bench in claim 3, wherein said test case utilizes the same software driver to configure and control said SOC interface and said verification interface model.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

14. In regards to Claim 5, Blaner teaches the following limitations:

5.The verification test bench in claim 3, wherein said test case utilizes different software drivers to configure and control said SOC interface and said verification interface model.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU) controls up to eight banks of mixed types of memories*** and operates at one-half the PLB [processor local bus] clock frequency. ... Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories."

15. In regards to Claim 6, Blaner teaches the following limitations:

6. The verification test bench system in claim 1, wherein said verification interface model tests an operational capability of said SOC interface.

(2) Blaner teaches (See "E. Verification Testbench"): "System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench."

16. In regards to Claim 7, Blaner teaches the following limitations:

7. The verification test bench system in claim 1, further comprising at least one additional verification interface model connected to said test bench EBIU for testing additional types of SOC interfaces.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

17. In regards to Claim 8, Blaner teaches the following limitations:

8. A verification test bench system for testing a system-on-a-chip (SOC) interface of an SOC, said verification test bench system comprising:

a verification interface model connected to said SOC interface; and

(See Blaner, especially: p.208, "E. Verification Testbench")

Blaner teaches (See "E. Verification Testbench". Emphasis added): "To accomplish this synchronization, ***a memory-mapped external device*** containing software readable and writable registers that appear as wires in the testbench ***is connected to the external bus***."

a test bench external bus interface unit (EBIU) connected to said verification interface model,

wherein said test bench EBIU is connected to a SOC EBIU within said SOC, and

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

Moreover, Fig.2 of Blaner (see p.205), shows an EBIU in the extreme upper-left corner of the SOC block diagram. This diagram shows that the SOC EBIU connects externally to "SRAM, Flash, ROM, and 'External Master'".

While Blaner does not expressly teach that the "off-chip device, called the external bus master" also uses an EBIU in order to connect to the SOC's EBIU, examiner finds this to be inherent because:

(1) The two ends of an interface must match (e.g. electrical plug and socket, phone jack and socket, parallel port plugs and sockets, etc.), otherwise the interface does not work properly. This applies also to the external buses on SOCs, and

(2) Blaner teaches (See "E. Verification Testbench"): "System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench." A complete system verification must also include a verification of the EBIU on the SOC, therefore the testbench must have an interface compatible with the SOC EBIU.

wherein said test bench EBIU and said SOC EBIU are mastered by the same processor in said SOC.

(See Blaner, especially: p.208, "E. Verification Testbench")

Blaner teaches (See "E. Verification Testbench". Emphasis added): "Wrap backs are utilized as much as possible, and behaviorals often contain hard-coded packet or stream data."

Examiner interprets that "Wrap backs" do not containing functioning processors, and therefore must rely on the SOC processor.

18. In regards to Claim 15, Blaner teaches the following limitations:

15. A verification test bench system for testing a system-on-a-chip (SOC) interface of an SOC, said verification test bench system comprising:

a verification interface model connected to said SOC interface; and

(See Blaner, especially: p.208, "E. Verification Testbench")

Blaner teaches (See "E. Verification Testbench". Emphasis added): "To accomplish this synchronization, ***a memory-mapped external device***

containing software readable and writable registers that appear as wires in the testbench ***is connected to the external bus***."

a test bench external bus interface unit (EBIU) connected to said verification interface model,

wherein said test bench EBIU is connected to a SOC EBIU within said SOC, and

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

Moreover, Fig.2 of Blaner (see p.205), shows an EBIU in the extreme upper-left corner of the SOC block diagram. This diagram shows that the SOC EBIU connects externally to "SRAM, Flash, ROM, and 'External Master'".

While Blaner does not expressly teach that the "off-chip device, called the external bus master" also uses an EBIU in order to connect to the SOC's EBIU, examiner finds this to be inherent because:

(1) The two ends of an interface must match (e.g. electrical plug and socket, phone jack and socket, parallel port plugs and sockets, etc.), otherwise the interface does not work properly. This applies also to the external buses on SOCs, and

(2) Blaner teaches (See "E. Verification Testbench"): "System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench." A complete system verification must also include a verification of the EBIU on the SOC, therefore the testbench must have an interface compatible with the SOC EBIU.

wherein said test bench EBIU and said SOC EBIU are mastered by the same processor in said SOC, such that said SOC interface and said verification interface model are programmed by the same test case running in said SOC.

(See Blaner, especially: p.208, "E. Verification Testbench")

Blaner teaches (See "E. Verification Testbench". Emphasis added): "Wrap backs are utilized as much as possible, and behaviorals often contain hard-coded packet or stream data."

Examiner interprets that "Wrap backs" do not containing functioning processors, and therefore must rely on the SOC processor.

19. In regards to Claim 21, Blaner teaches the following limitations:

21. A method of testing a system-on-a-chip (SOC) interface of an SOC, said method comprising:

connecting a verification interface model to said SOC interface;

(See Blaner, especially: p.208, "E. Verification Testbench")

Blaner teaches (See "E. Verification Testbench". Emphasis added): "To accomplish this synchronization, ***a memory-mapped external device*** containing software readable and writable registers that appear as wires in the testbench ***is connected to the external bus***."

connecting a test bench external bus interface unit (EBIU) to said verification interface model;

connecting said test bench EBIU to a SOC EBIU within said SOC; and comparing said SOC interface with said interface model.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

Moreover, Fig.2 of Blaner (see p.205), shows an EBIU in the extreme upper-left corner of the SOC block diagram. This diagram shows that the SOC EBIU connects externally to "SRAM, Flash, ROM, and 'External Master'".

While Blaner does not expressly teach that the "off-chip device, called the external bus master" also uses an EBIU in order to connect to the SOC's EBIU, examiner finds this to be inherent because:

(1) The two ends of an interface must match (e.g. electrical plug and socket, phone jack and socket, parallel port plugs and sockets, etc.),

otherwise the interface does not work properly. This applies also to the external buses on SOCs, and

(2) Blaner teaches (See "E. Verification Testbench"): "System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench." A complete system verification must also include a verification of the EBIU on the SOC, therefore the testbench must have an interface compatible with the SOC EBIU.

20. In regards to Claim 28, Blaner teaches the following limitations:

28. A program storage device readable by machine tangibly embodying a program of instructions executable by the machine to perform a method for testing a system-on-a-chip (SOC) interface of an SOC, said method comprising:

connecting a verification interface model to said SOC interface;

(See Blaner, especially: p.208, "E. Verification Testbench")

Blaner teaches (See "E. Verification Testbench". Emphasis added): "To accomplish this synchronization, ***a memory-mapped external device*** containing software readable and writable registers that appear as wires in the testbench ***is connected to the external bus***."

connecting a test bench external bus interface unit (EBIU) to said verification interface model;

connecting said test bench EBIU to a SOC EBIU within said SOC; and

comparing said SOC interface with said interface model.

(See Blaner, especially: p.205, "II. SOC Structure")

Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"

Moreover, Fig.2 of Blaner (see p.205), shows an EBIU in the extreme upper-left corner of the SOC block diagram. This diagram shows that the SOC EBIU connects externally to "SRAM, Flash, ROM, and 'External Master'".

> While Blaner does not expressly teach that the "off-chip device, called the external bus master" also uses an EBIU in order to connect to the SOC's EBIU, examiner finds this to be inherent because:
>
> (1) The two ends of an interface must match (e.g. electrical plug and socket, phone jack and socket, parallel port plugs and sockets, etc.), otherwise the interface does not work properly. This applies also to the external buses on SOCs, and
>
> (2) Blaner teaches (See "E. Verification Testbench"): "System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench." A complete system verification must also include a verification of the EBIU on the SOC, therefore the testbench must have an interface compatible with the SOC EBIU.

21. Dependent Claims 2, 9, 16, 22, and 29 differ only in the limitations that they inherit from their parent claims. Therefore Claims 9, 16, 22, and 29 are rejected for the same reasons as claim 2, in combination with the rejections of their respective parent claims, which are recited above.

22. Dependent Claims 3, 10, 23, and 30 differ only in the limitations that they inherit from their parent claims. Therefore Claims 10, 23, and 30 are rejected for the same reasons as claim 3, in combination with the rejections of their respective parent claims, which are recited above.

23. Dependent Claims 4, 11, 17, 24, and 31 differ only in the limitations that they inherit from their parent claims. Therefore Claims 11, 17, 24, and 31 are rejected for the same reasons as claim 4, in combination with the rejections of their respective parent claims, which are recited above.

24. Dependent Claims 5, 12, 18, 25, and 32 differ only in the limitations that they inherit from their parent claims. Therefore Claims 12, 18, 25, and 32 are rejected

for the same reasons as claim 5, in combination with the rejections of their respective parent claims, which are recited above.

25. Dependent Claims 6, 13, 19, 26, and 33 differ only in the limitations that they inherit from their parent claims. Therefore Claims 13, 19, 26, and 33 are rejected for the same reasons as claim 6, in combination with the rejections of their respective parent claims, which are recited above.

26. Dependent Claims 7, 14, 20, 27, and 34 differ only in the limitations that they inherit from their parent claims. Therefore Claims 14, 20, 27, and 34 are rejected for the same reasons as claim 7, in combination with the rejections of their respective parent claims, which are recited above.

27. Claims 1-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Devins.

28. In regards to Claim 1, Devins teaches the following limitations:

1. A verification test bench system for testing a system-on-a-chip (SOC) interface of an SOC, said verification test bench system comprising:

a verification interface model connected to said SOC interface; and

a test bench external bus interface unit (EBIU) connected to said verification interface model,

wherein said test bench EBIU is connected to a SOC EBIU within said SOC.

The "external bus interface logic" in the "device is coupled to said system-on-chip device via a chip-external bus" that is claimed in claim 18 of the issued Devins patent is enabled in the specification of that patent in Fig.2, Item 202, and further in column 4, lines 15-20 and 38-40, as well as col.5, lines 5-8. This

corresponds to the "test bench external bus interface unit (EBIU)" claimed in claims 1, 8, and 15 of the instant application.

While the issued patent does not expressly teach that the "system-on-chip" device also uses an EBIU in order to connect to the test unit's EBIU, Examiner finds this to be inherent because the two ends of an interface must match (e.g. electrical plug and socket, phone jack and socket, parallel port plugs and sockets, etc.), otherwise the interface does not work properly. This reasoning is especially relevant because the issued patent teaches (See col.4, lines 15-20):

> The external bus interface logic 202 is designed to direct signals received via connection 107 to the appropriate logical address, and to convert the particular bus protocol received into an internally-used format applicable to the command decode logic 203.

29. In regards to Claim 2, Devins teaches the following limitations:

> 2.The verification test bench system in claim 1, wherein said SOC EBIU allows a test case running in said SOC to control both said SOC interface and said verification interface model.

(See Devins patent, especially: Fig.2, Item 202, and further in column 4, lines 15-20 and 38-40, as well as col.5, lines 5-8)

30. In regards to Claim 3, Devins teaches the following limitations:

> 3.The verification test bench system in claim 1, wherein said SOC interface and said verification interface model are programmed by a test case running in said SOC.

(See Devins patent, especially: Fig.2, Item 202, and further in column 4, lines 15-20 and 38-40, as well as col.5, lines 5-8)

31. In regards to Claim 4, Devins teaches the following limitations:

> 4.The verification test bench in claim 3, wherein said test case utilizes the same software driver to configure and control said SOC interface and said verification interface model.

(See Devins patent, especially: Fig.2, Item 202, and further in column 4, lines 15-20 and 38-40, as well as col.5, lines 5-8)

32. In regards to Claim 5, Devins teaches the following limitations:

> 5.The verification test bench in claim 3, wherein said test case utilizes different software drivers to configure and control said SOC interface and said verification interface model.

(See Devins patent, especially: Fig.2, Item 202, and further in column 4, lines 15-20 and 38-40, as well as col.5, lines 5-8)

33. In regards to Claim 6, Devins teaches the following limitations:

> 6. The verification test bench system in claim 1, wherein said verification interface model tests an operational capability of said SOC interface.

(See Devins patent, especially: Fig.2, Item 202, and further in column 4, lines 15-20 and 38-40, as well as col.5, lines 5-8)

34. In regards to Claim 7, Devins teaches the following limitations:

> 7. The verification test bench system in claim 1, further comprising at least one additional verification interface model connected to said test bench EBIU for testing additional types of SOC interfaces.

(See Devins patent, especially: Fig.2, Item 202, and further in column 4, lines 15-20 and 38-40, as well as col.5, lines 5-8)

35. Independent Claims 8, 15, 21, and 28 are rejected on the same grounds as independent claim 1.

36. Dependent Claims 2, 9, 16, 22, and 29 differ only in the limitations that they inherit from their parent claims. Therefore Claims 9, 16, 22, and 29 are rejected for the same reasons as claim 2, in combination with the rejections of their respective parent claims, which are recited above.

37. Dependent Claims 3, 10, 23, and 30 differ only in the limitations that they inherit from their parent claims. Therefore Claims 10, 23, and 30 are rejected for the same reasons as claim 3, in combination with the rejections of their respective parent claims, which are recited above.

38. Dependent Claims 4, 11, 17, 24, and 31 differ only in the limitations that they inherit from their parent claims. Therefore Claims 11, 17, 24, and 31 are rejected

for the same reasons as claim 4, in combination with the rejections of their respective parent claims, which are recited above.

39. Dependent Claims 5, 12, 18, 25, and 32 differ only in the limitations that they inherit from their parent claims. Therefore Claims 12, 18, 25, and 32 are rejected for the same reasons as claim 5, in combination with the rejections of their respective parent claims, which are recited above.

40. Dependent Claims 6, 13, 19, 26, and 33 differ only in the limitations that they inherit from their parent claims. Therefore Claims 13, 19, 26, and 33 are rejected for the same reasons as claim 6, in combination with the rejections of their respective parent claims, which are recited above.

41. Dependent Claims 7, 14, 20, 27, and 34 differ only in the limitations that they inherit from their parent claims. Therefore Claims 14, 20, 27, and 34 are rejected for the same reasons as claim 7, in combination with the rejections of their respective parent claims, which are recited above.

Response to Arguments

42. Applicant's arguments filed 11/23/2005 have been fully considered but they are not persuasive.

43. Regarding the Blaner reference, Applicants unpersuasively argue (see p.10 of Applicants' arguments filed 11/23/2005) that it does not disclose:

> ***connecting the testbench to an external SOC via the SOC interface and the model interface (independent claims 1, 8, 15, 21, and 28).***

44. In response, Examiner notes that Blaner expressly teaches the following (see p.208, Section E. "Verification Testbench". Emphasis added):

> System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench. ...
>
> Because testcases are self-checking, all external activity is synchronized to the internal software. To accomplish this synchronization, ***a memory-mapped external device*** containing software readable and writable registers that appear as wires in the testbench ***is connected to the external bus.*** Verliog models accept the wires as triggers and respond with status on the wires.
>
> The testbench also utilizes a memory-mapped Verilog device, known as the external messaging unit (EMU), for displaying time-stamped trace and status information to users via the simulation console.

Blaner also teaches (see p.207, Section IV "Design Verification". Emphasis added):

> ***The SOC was verified using a software-based verification system.*** A system exerciser approach was used, which consists of a group of software test programs linked together by a group of software test programs linked together by a special verification operating system called the Test Operating System (TOS) [1]. ***TOS is capable of scheduling test programs for execution and multi-tasking operations, enabling concurrent core execution. This provides the appropriate intercore and bus transactions required for exercising the chip.***

Blaner also teaches (see p.205, "II. SOC Structure". Emphasis added):

> Blaner teaches (See "II. SOC Structure". Emphasis added): "... ***The external bus interface unit (EBIU)*** controls up to eight banks of mixed types of memories and operates at one-half the PLB [processor local bus] clock frequency. ... ***Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.***"
>
> Moreover, Fig.2 of Blaner (see p.205), shows an EBIU in the extreme upper-left corner of the SOC block diagram. This diagram shows that the

SOC EBIU connects externally to "SRAM, Flash, ROM, and 'External Master'".

While Blaner does not expressly teach that the "off-chip device, called the external bus master" also uses an EBIU in order to connect to the SOC's EBIU, examiner finds this to be inherent because:

(1) The two ends of an interface must match (e.g. electrical plug and socket, phone jack and socket, parallel port plugs and sockets, etc.), otherwise the interface does not work properly. This applies also to the external buses on SOCs, and

(2) Blaner teaches (See "E. Verification Testbench"): "System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench." A complete system verification must also include a verification of the EBIU on the SOC, therefore the testbench must have an interface compatible with the SOC EBIU.

45. Examiner therefore strongly disagrees with the Applicants' argument that "nothing in Blaner mentions connecting the testbench to an external SOC via the SOC interface and the model interface." (see p.10 of Applicants' arguments). In particular, the above cited sections of Blaner expressly teach:

a. Connecting the text bench to an external SOC ("*<u>The SOC was verified using a software-based verification system</u>*." Blaner, p.207, Section IV "Design Verification").

b. Connecting the text bench to an external SOC via an SOC interface ("*<u>Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories.</u>*" Blaner, p.205, "II. SOC Structure").

c. Connecting the testbench to an external SOC via the SOC interface and the model interface. ("*<u>TOS is capable of scheduling test programs for</u>*

execution and multi-tasking operations, enabling concurrent core execution. This provides the appropriate intercore and bus transactions required for exercising the chip." Blaner, p.207, Section IV "Design Verification").

46. Regarding the Blaner reference, the Applicants also unpersuasively argue (see p.11 of Applicants' arguments filed 11/23/2005) that it does not disclose:

> ***a test case in the SOC that can use the same software driver to program both the SOC interface and the model interface (dependent claims 4, 11, 17, 24, and 31).***

47. In response, Examiner notes that in addition to the above cited sections of the Blaner reference, Blaner also teaches the following (see p.207, Section IV "Design Verification", Sub-section D "TOS Structure". Emphasis added):

> The TOS [Test Operating System] system consists of a set of self-checking test programs written in C and linked together to operate independently of one another ...The system is constructed hierarchically from the top down, as shown in Fig.3. ... The top layer is called the chip exerciser, the middle contains the set of test application programs, and the bottom is where device drivers reside.
>
> One motivation behind this hierarchical layering is to promote software reusability: isolating chip-specific details in the exerciser enables reuse of application and driver code on other chips.

Examiner also notes that Fig.3 on p.207 shows a hierarchy of "User Interface & Chip Exerciser", "Test Application", "Device Driver", and "Core". The first paragraph of Section II "SOC Structure" on p.205 teaches that "PLB and OPB are two of the three IBM CoreConnect buses", indicating that the cores are components on the SOC. The first paragraph of Section II.B "OPB Subsystem" on p.206 confirms this definition with the teaching that "The OPB interconnects

lower-performance cores to the PLB through the PLB-OPB bridge and HSDMA ..."

48. Examiner also disagrees with the Applicants' argument that "nothing in Blaner mentions a test case in the SOC that can use the same software driver to program both the SOC interface and the model interface." (see p.12 of Applicants' arguments). In particular, Figure 3, and its associated text in Sections II.D and II.E teach that the same test application is used to program both the device driver and the core. This encompasses the claimed "verification interface model" and "SOC interface".

Moreover, as cited earlier in this Office Action, Blaner teaches in Section II.E that

> System verification requires stimulus/expectation models or devices to be attached to the external interfaces of the chip. Such models are often implemented in a testbench. ...
>
> Because testcases are self-checking, all external activity is synchronized to the internal software. To accomplish this synchronization, a memory-mapped external device containing software readable and writable registers that appear as wires in the testbench is connected to the external bus. Verliog models accept the wires as triggers and respond with status on the wires.
>
> The testbench also utilizes a memory-mapped Verilog device, known as the external messaging unit (EMU), for displaying time-stamped trace and status information to users via the simulation console.

49. Regarding the Devins reference, Applicants unpersuasively argue (see pp.10-11 of Applicants' arguments filed 11/23/2005) that it does not disclose:

> ***connecting the testbench to an external SOC via the SOC interface and the model interface (independent claims 1, 8, 15, 21, and 28).***

> ***a test case in the SOC that can use the same software driver to program both the SOC interface and the model interface (dependent claims 4, 11, 17, 24, and 31).***

50. In response, Examiner notes that Devins expressly teaches the following (see col.2, lines 15-43. Emphasis added):

> However, inefficiencies in current verification methodologies exacerbate time pressures. For example, SOC designs typically interface with cores that are external to the design. Existing methods of including such external cores in a verification test of a SOC design typically entail having to create special test cases to control the external cores; such test cases typically do not communicate with test cases being applied internally to the SOC and therefore lack realism. Calls to built-in simulator functions to control external cores are also used. However, such an approach is simulator-dependent and therefore not portable across simulators.
>
> A verification methodology is needed which addresses the problems noted in the foregoing, which represent factors extending time-to-market.
>
> SUMMARY OF THE INVENTION
>
> The present invention provides a method for communicating with and controlling cores which are external to a SOC design during verification of the design, which avoids the above-noted inefficiencies in existing verification methods. ***<u>According to the method, an external memory-mapped test device (EMMTD) is coupled between a SOC design being tested in simulation, and cores external to the SOC design.</u>*** The EMMTD is coupled to the SOC via a chip-external bus, and coupled to external cores, or to the external interfaces of cores internal to the SOC, via an EMMTD bi-directional bus.
>
> The EMMTD processes signals received over the chip external bus and applies them to an external core, or to an internal core with an external interface, coupled to the EMMTD bi-directional bus. Internal logic in the EMMTD provides for control and status monitoring of a core coupled to the EMMTD bi-directional bus by enabling functions including driving data on the bus, reading the current state of data on the bus, and capturing positive and negative edge transitions on the bus.

> ***A test case being executed for SOC verification by a simulated embedded processor in the SOC can communicate with and control elements external to the SOC, by using the EMMTD to perform such functions as initiating external core logic which drives test signals to an internal core, directly controlling an internal core via its external interface, or determining the status of an external core.***
>
> The EMMTD may also be physically embodied in, for example, an FPGA (Field Programmable Gate Array) or an ASIC (Application Specific Integrated Circuit) usable with real hardware.

51. Examiner therefore finds that the Devins reference teaches the claimed limitations.

Conclusion

52. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

53. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749.

Any response to this office action should be faxed to (571) 273- 8300, or mailed to:

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or hand carried to:

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Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon
Art Unit 2123
February 7, 2006

Paul L. Rodriguez 2/8/06
Primary Examiner
Art Unit 2125